

REMARKS

The dependencies of claims 8 and 24 have been amended so they now depend on their respected independent claims. Withdrawal of the objection to these claims is respectfully requested.

Claims 1-2, 6, 8-9, 11-18, 22, 24, 25, and 27-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over previously-cited applied DeRoo et al. in view of newly-applied U.S. Patent 5,363,334 to Alexander et al. This rejection is respectfully traversed.

DeRoo fails to teach irreversible blocking of subsequent writing of data into a protected part of memory after data is initially stored there. DeRoo protects writing to a protected address range using a gating mechanism. The statement in column 88, line 6, "when the block protection feature is enabled," makes clear there are times when the block protection feature may be disabled to permit writing to that boot block. Moreover, by manipulating the values of HUICFG_1, one may readily change the memory contents of the particular area being protected. Accordingly, and as admitted by the Examiner, the previously-protected area can be written to in DeRoo. Hence, there is no irreversible blocking.

In an effort to remedy this deficiency, the Examiner now turns to the Alexander patent. As explained in conjunction with Figure 7, a register A is used to store the address of the first block to be write-protected. Register B is used to store the number of contiguous blocks to be write-protected. Registers A and B are rendered inaccessible to

prevent alteration of either the security start block address or the number of contiguous blocks secured. Specifically, one or more sets of block-out fuses are "blown" to open the data paths to registers A and B. In practice, each block-out fuse is modelled by a one bit register C that may be set or cleared by writing an appropriate bit to that register. Any subsequent attempt to rewrite the bits in registers A and B is prevented by the state of register C.

It is not clear whether the security register C irreversibly blocks subsequent writing of data into a protected area of memory. Indeed, the one-bit register C is described in Alexander as being alterable: "each lockout fuse is modeled by a one bit register (e.g., register C of Fig. 7) that may be set or cleared by writing an appropriate bit to the register." Column 7, lines 19-22. This language suggests that a set register C in the secure state may be cleared to permit subsequent writing to the portions of memory designated by registers A and B. Hence, those portions of memory protected are not irreversibly blocked from subsequent writing. Accordingly, Alexander does not remedy DeRoo's deficiency.

But even if Alexander described register C as being physically unalterable after being set to effect irreversible blocking of subsequent writing into protected portion of memory, it would be inconsistent to combine such a teaching with DeRoo. As already described, a basic premise in DeRoo is to allow data writing into a protected memory portion. To modify DeRoo so that premise is destroyed renders DeRoo inoperable for its intended purpose. The Federal Circuit has admonished that a modification of a reference

which renders it inoperable for its intended is inappropriate for purposes of an obviousness rejection. *In re Fritch* 972 F.2d 1260, 1265-1266 (Fed. Cir. 1992). A similar finding was made in *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984). The combination of DeRoo and Alexaner is improper.

Accordingly, Applicants respectfully submit that the rejections based upon DeRoo and Alexander should be withdrawn. Moreover, the rejection of certain dependent claims is also believed to be improper for additional reasons.

For example, the Examiner contends that Alexander teaches the features of claims 8 and 24. Particularly, the Examiner contends that Alexander discloses that the "write line is permanently interrupted," reading this language on an address comparison operation. Applicants have reviewed the text in Alexander at column 2, lines 44-48 and find no teaching of a "write line" in Alexander's EEPROM being "permanently interrupted." Indeed, even when register C is set, it is the data paths to registers A and B which are physically interrupted. A write line used to write data into a specific part of memory is not physically interrupted. In other words, registers A and B in Alexander are not part of the protected portion of memory.

Regarding claims 9 and 25, the write line, which is a fusable link in the claims, is not a line used to write to the registers A and B, but rather a write line to write into a protective part of the memory. See for example the first step in claims 8 and 24 from which claims 9 and 25 respectively depend.

Regarding dependent claim 16, the Examiner fails to point out where DeRoo discloses that the communication device is a "bluetooth communication device."

Claims 10 and 26 stand rejected under 35 U.S.C. §103 as being unpatentable over DeRoo in view of Alexander and further in view of U.S. Patent 5,546,561 to Kynett et al. This rejection is respectfully traversed.

The Examiner refers to column 6, lines 1-7 which describe a write state machine which controls a write path and verification circuitry of a memory array 22. Although the write state machine 32 may control times when the memory may be programmed or erased, there is no teaching in Kynett that the write state machine 32 protects the nonvolatile memory to the extent that subsequent writing to a protected part is irreversibly blocked.

The Examiner alleges it would have been obvious to combine the teachings of Kynett with both DeRoo and Alexander because Kynett's state machine "will simplify the process by deceasing [sic] the system throughput," referring to column 2, lines 47-57. Applicants have reviewed this text in column 2 and find no support for the Examiner's contention that the Kynett's state machine would simplify protecting memory from being written into by decreasing system throughput.

Claims 3-5, and 19-21 stand rejected under 35 U.S.C. §103 as being unpatentable over DeRoo, Alexander, and further in view of U.S. Patent 6,401,208 to Davis et al. This rejection is respectfully traversed.

Davis discloses embedding a BIOS certificate and a BIOS signature in the BIOS code in order to authenticate the BIOS code. During an authentication process, the BIOS certificate is decrypted using the root certification key to retrieve a public key of the BIOS signature. Various processings are then performed based on this cryptographic information to determine if there is a match. If the match occurs, the BIOS code has been authenticated. If not, there is no authentication. In contrast, claims 4 and 20 recite "calculating a characteristic parameter for data being checked for changes" in a portion of the memory. In contrast, Davis' system simply determines whether the certification information matches and whether the BIOS code is authentic. No determination is made whether the BIOS code has been changed. The Examiner contends that the characteristic parameter is a checksum, as claimed in claims 5 and 21, and refers generically to Figure 6B in Davis. While there are various cryptographic operations are performed, Applicants find no explicit teaching of a checksum being calculated to check for changes in a portion of memory in Figure 6B in Davis.

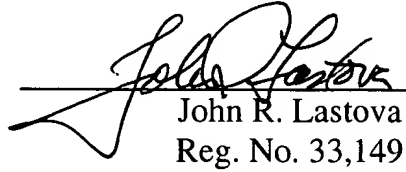
Applicants respectfully submit that the present application is condition for allowance. An early notice to that effect is earnestly solicited.

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Respectfully submitted,

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